HB2200

Innovative IEEE 802.15.4/ZigBee compatible SoC
for massive IoT networking

Datasheet

DS-HB2200

Version 1.0

Revision History

Revision No.	Date	Description	
1.0	Dec. 11, 2019	• Initial release	

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1. HB2200 SoC overview

1.1. Description

HB2200 is an innovative "IoT connectivity" system-on-chip (SoC) enabling secure construction of low-power large-scale IoT networks in 2.4 GHz ISM band. It is equipped with a built-in *hy*Bee MAC and networking engine (MaNE) that innovatively resolves major drawbacks of IEEE 802.15.4 and ZigBee, while providing full backward compatibility with them. The built-in *hy*Bee MaNE supports self-network construction in a multi-hop structure, while. Its robustness to interference provides quite stable network operation even in harsh interference environments, while keeping the power consumption of HB2200 little changed. Note that conventional IoT connectivity technologies (e.g., ZigBee, Bluetooth, BLE and Z-Wave) may suffer from large increase of power consumption in the presence of interference. The *hy*Bee MaNE also provides very fast and energy efficient self-healing capability. HB2200 can easily be applied to low-power IoT service environments in a plug-and-play mode, where conventional IoT connectivity technologies cannot.

1.2. Features

- CPU
  - ARM Cortex-M0 32-bit core processor
  - Nested vectored interrupt controller
  - Serial wire debug (SWD)

- Memory allocation
  - 128 Kbytes embedded flash memory to store code/data
  - 32 Kbytes SRAM for general purpose

- Embedded flash memory
  - Page 2 Kbytes erase and double word (4 bytes) program
    - ✓ Program time: 20/40 us (min./max.)
    - ✓ Erase time: 20/40 ms (min./max.)
  - Endurance: 20,000 cycles (min.)
  - Data retention: 100 years under room temperature

- System and interface peripherals
  - 2 SPIs (master and slave)
  - 2 UARTs
  - 4 timer/PWMs
  - 21 GPIOs
  - ADC

- 2.4 GHz IEEE 802.15.4 compliant RF transceiver
  - 2.4 GHz O-QPSK 802.15.4 with 250 Kbps data rate
  - Programmable Tx output power from 0 dBm to -40 dBm
  - Integrated low phase noise VCO, frequency synthesizer and PLL loop filter
  - Receiver sensitivity of -95 dBm and 3 dBm max. input level
  - Integrated RSSI ADC and I/Q DACs

- Security functions
  - AES-128 for data encryption
  - True random number generator (TRNG)

- *hy*Bee MAC and network engine (MaNE)
  - Full backward compatibility with IEEE 802.15.4/ZigBee
  - Tree-structured self-networking of up to 2,000+ nodes

- Stable multi-hop operation with low signaling overhead
- High network scalability in multi-hop networking environments
- Stable performance even in the presence of harsh interference
- Low power operation even in harsh operation environments
- Fast and energy efficient network recovery
- Reduced packet collision in high-density network environments
- Alleviation of hidden node problem
- Over-the-air (OTA) firmware upgrade support

- Clock generation
  - External clock sources
    - ✓ 32 MHz crystal oscillator
    - ✓ 32.768 KHz crystal oscillator
  - Internal clock sources
    - ✓ 32 MHz RC oscillator
    - ✓ 32.768 KHz RC oscillator

- Operating characteristics
  - Operating voltage: 3.0 V ~ 3.6 V
  - Operating temperature: -40 °C to 85 °C
  - ESD HBM 2 KV, CDM 500 V

- Package
  - 68-QFN package
  - 8.0 mm x 8.0 mm x 0.75 mm dimension
  - Lead pitch 0.4 mm

- Development kit (DK2200)
  - Keil uVision
  - Software development kit
  - Evaluation board (EVB2200)
  - Reference design kit

- Application areas, but not limited to
  - Smart lighting control in a large scale
  - Smart building system (SBS)
  - Smart farming
  - Parking lot management system
  - Factory management systems
  - Smart hospital and healthcare
  - Smart home
  - Electronic shelf labeling (ESL)
  - Battery management system (BMS)
  - Street lighting
  - Smart logistics
  - Wireless control of automotive devices

1.3. Functional block diagram

As illustrated in Figure 1-1, HB2200 SoC comprises ARM Cortex-M0 32-bit core processor, IEEE 802.15.4/ZigBee 2.4 GHz RF transceiver, 32 Kbytes SRAM, 128 Kbytes embedded flash memory, power management blocks, security engines and analog/digital interfaces.

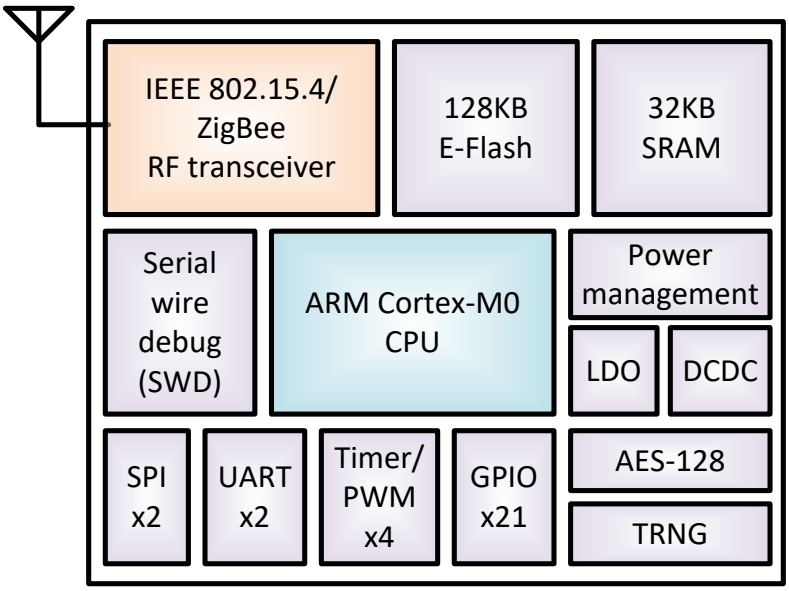

Figure 1-1. Block diagram of HB2200 SoC

2. Pin description

2.1. Package outline

Figure 2-1 depicts the package outline of HB2200 SoC.

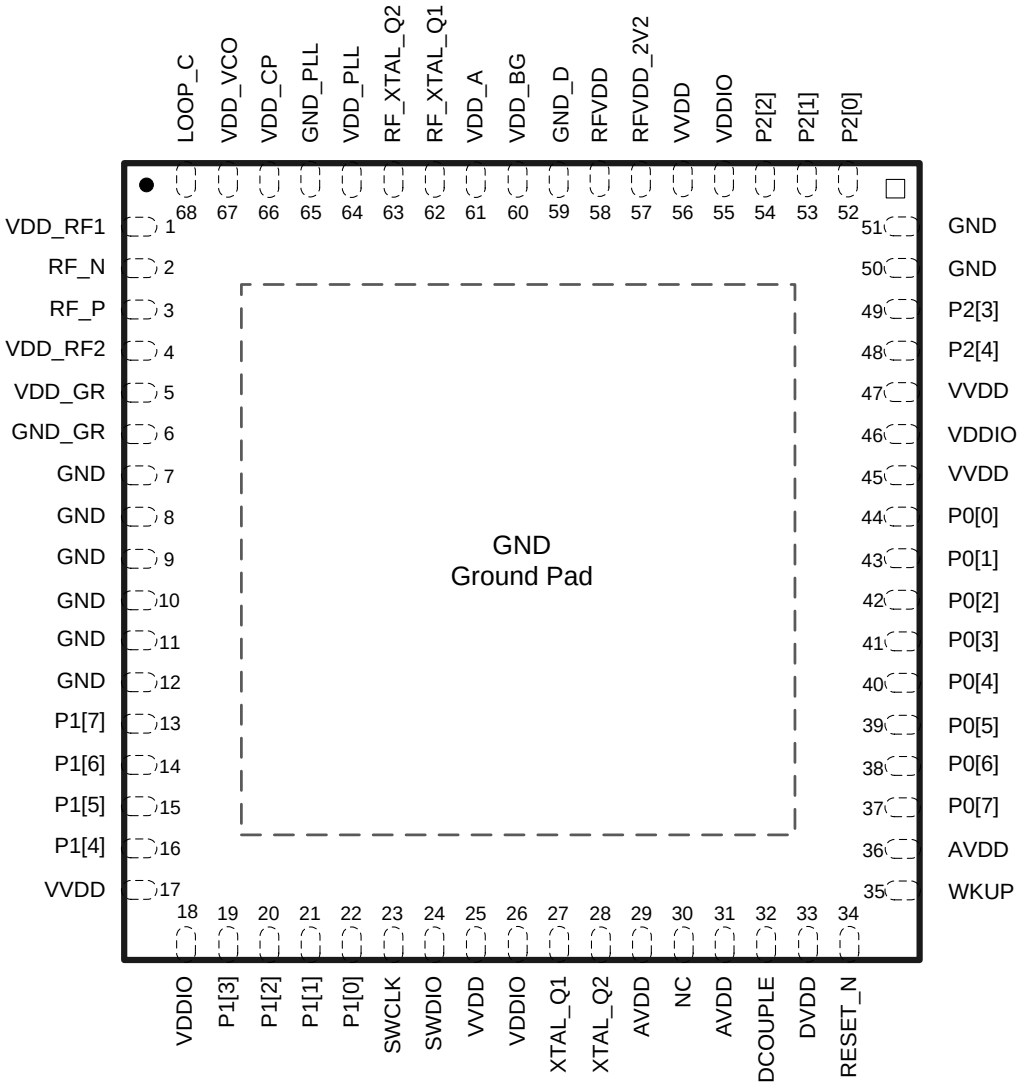

Figure 2-1. Package outline of HB2200 SoC

2.2. Pin description

Table 2-1. Pin description of HB2200 SoC

NO.	NAME	TYPE	DESCRIPTION
1	VDD_RF1	Power	RF power supply (3.3V)
2	RF_N	RF input	Negative RF input signal
3	RF_P	RF input	Positive RF input signal
4	VDD_RF2	Power	RF power supply (3.3V)
5	VDD_GR	Power	RF guard ring power supply (3.3V)
6	GND_GR	Ground	RF guard ring ground
7	GND	-	Connect to GND
8	GND	-	Connect to GND
9	GND	-	Connect to GND

10	GND	-	Connect to GND
11	GND	-	Connect to GND
12	GND	-	Connect to GND
13	P1[7]	Digital I/O	Port 1.7
14	P1[6]	Digital I/O	Port 1.6
15	P1[5]	Digital I/O	Port 1.5
16	P1[4]	Digital I/O	Port 1.4
17	VVDD	Power	Digital core power supply (1.8V)
18	VDDIO	Power	I/O power supply (3.3V)
19	P1[3]	Digital I/O	Port 1.3
20	P1[2]	Digital I/O	Port 1.2
21	P1[1]	Digital I/O	Port 1.1
22	P1[0]	Digital I/O	Port 1.0
23	SWCLK	Digital I/O	Serial wire clock
24	SWDIO	Digital I/O	Serial wire debug data input/output
25	VVDD	Power	Digital core power supply (1.8V)
26	VDDIO	Power	I/O power supply (3.3V)
27	XTAL_Q1	XTAL	32 MHz crystal oscillator pin 1
28	XTAL_Q2	XTAL	32 MHz crystal oscillator pin 2
29	AVDD	Power	Analog power supply (3.3V)
30	NC	-	Open
31	AVDD	Power	Analog power supply (3.3V)
32	DCOUPLE	Power output	LDO output (1.8V)
33	DVDD	Power input	LDO power supply (3.3V)
34	RESET_N	Digital input	Reset, active-low
35	WKUP	Analog input	Wake-up interrupt, active-high
36	AVDD	Power	Analog power supply (3.3V)
37	P0[7]	Digital/Analog I/O	Port 0.7
38	P0[6]	Digital/Analog I/O	Port 0.6
39	P0[5]	Digital/Analog I/O	Port 0.5
40	P0[4]	Digital/Analog I/O	Port 0.4
41	P0[3]	Digital/Analog I/O	Port 0.3
42	P0[2]	Digital/Analog I/O	Port 0.2
43	P0[1]	Digital/Analog I/O	Port 0.1
44	P0[0]	Digital/Analog I/O	Port 0.0
45	VVDD	Power	Digital core power supply (1.8V)
46	VDDIO	Power	I/O power supply (3.3V)
47	VVDD	Power	Digital core power supply (1.8V)
48	P2[4]	Digital/Analog I/O	Port 2.4, 32.768 KHz crystal oscillator pin 2
49	P2[3]	Digital/Analog I/O	Port 2.3, 32.768 KHz crystal oscillator pin 1
50	GND	-	Connect to GND
51	GND	-	Connect to GND
52	P2[0]	Digital I/O	Port 2.0
53	P2[1]	Digital I/O	Port 2.1
54	P2[2]	Digital I/O	Port 2.2
55	VDDIO	Power	I/O power supply (3.3V)
56	VVDD	Power	Digital core power supply (1.8V)
57	RFVDD_2V2	Power output	RF DC-DC output
58	RFVDD	Power input	RF DC-DC input and misc. block power supply (3.3V)
59	GND_D	Ground	RF digital ground
60	VDD_BG	Power	RF bandgap power supply (3.3V)
61	VDD_A	Power	RF analog power supply (3.3V)
62	RF_XTAL_Q1	Analog I/O	32 MHz crystal oscillator pin 1 for RF
63	RF_XTAL_Q2	Analog I/O	32 MHz crystal oscillator pin 2 for RF
64	VDD_PLL	Power	RF PLL power supply (3.3V)
65	GND_PLL	Ground	RF PLL ground
66	VDD_CP	Power	RF power supply (3.3V)
67	VDD_VCO	Power	RF power supply (3.3V)
68	LOOP_C	Analog input	RF PLL loop filter

2.3. GPIO assignments

HB2200 provides 21 GPIOs comprising P0, P1 and P2, each of which has a size of 8 bits, 8 bits and 5 bits, respectively. Each GPIO has multiple functionalities, which can be chosen by configuring the alternative function (AF). Table 2-2 summarizes the GPIO functions according to the AF configuration. All GPIO pins can be set as an input pull-up or pull-down (default: normal input).

Table 2-2. HB2200 GPIO muxing table

PIN NAME	PIN NO.	ALTERNATIVE FUNCTION (AF)							
		DIGITAL							ANALOG
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
P0[0]	44					PWM2			Ain0/[+]
P0[1]	43								Ain1/[-]
P0[2]	42		SPI1_MISO	UART0_RX	SPI2_CS				Ain2/[o]
P0[3]	41		SPI1_MOSI	UART0_TX	SPI2_CLK				Ain3
P0[4]	40		SPI1_CS		SPI2_MOSI	UART1_TX			Ain4/(-)
P0[5]	39		SPI1_CLK		SPI2_MISO	UART1_RX			Ain5/(+)
P0[6]	38					PWM0			Ain6
P0[7]	37								Ain7
P1[0]	22				PWM3				N/A
P1[1]	21					PWM0			N/A
P1[2]	20		SPI1_CS			PWM2			N/A
P1[3]	19		SPI1_CLK						N/A
P1[4]	16		SPI1_MISO	UART0_RX	SPI2_CS				N/A
P1[5]	15		SPI1_MOSI	UART0_TX	SPI2_CLK				N/A
P1[6]	14				SPI2_MOSI	UART1_TX			N/A
P1[7]	13				SPI2_MISO	UART1_RX			N/A
P2[0]	52					PWM3			N/A
P2[1]	53			UART0_RX		PWM2			N/A
P2[2]	54		PWM0	UART0_TX					N/A
P2[3]	49								Q1 (32 KHz)
P2[4]	48								Q2 (32 KHz)

3. System memory map

The memory configuration of HB2200 SoC is summarized in Table 3-1.

Table 3-1. System memory map of HB2200 SoC

System register (4KB)	0x4001_FFFF 0x4001_0000
Subsystem peripherals (64KB)	0x4000_FFFF 0x4000_0000
Reserved	0x3FFF_FFFF 0x0020_8000
SRAM (32KB)	0x0020_7FFF 0x0020_0000
Reserved	0x001F_FFFF 0x0010_0000
eFlash (128KB)	0x000F_FFFF 0x0000_0000

4. Electrical specification

ABSOLUTE MAXIMUM RATINGS(1)

		MIN	MAX	UNIT
Supply voltage (VDD)	All supply pins must have the same voltage	0	3.6	V
Voltage on any digital pin		0	VDD	V
ESD(2)	All pads, according to human-body model, JEDEC STD 22, method A114		2000	V
	According to charged-device model, JEDEC STD 22, method C101		500	V
Storage temperature		-40	125	˚C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) CAUTION: ESD sensitive device. Precaution should be required when handling the device in order to prevent permanent damage.

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
Operating ambient temperature range, T_A	-40	85	˚C
Operating supply voltage	3.0	3.6	V

ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Core current consumption	32 MHz XOSC running, no radio or peripherals active. Medium CPU activity: normal flash access, no RAM access		TBD		mA
	32 MHz XOSC running, radio in RX mode (waiting for signal), no peripherals active, CPU idle		TBD		mA
	32 MHz XOSC running, radio in TX mode, 0 dBm output power, no peripherals active, CPU idle		TBD		mA
	Power mode 1. Digital regulator on; 32 MHz RCOSC and 32 MHz crystal oscillator off; 32.768 KHz XOSC, POR, BOD and sleep timer active; RAM and register retention		TBD		mA
	Power mode 2. Digital regulator off; 32.768 KHz RCOSC running; comparator active		TBD		uA

GENERAL CHARACTERISTICS

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
RADIO PART					
RF frequency range	As defined by IEEE Std.802.15.4-2006	2405		2480	MHz
Radio baud rate	As defined by IEEE Std.802.15.4-2006		250		Kbps
Radio chip rate	As defined by IEEE Std.802.15.4-2006		2000		MChip/s
FLASH PART					
Flash erase time		20		40	ms
Flash page size			2		Kbytes

RF RECEIVE SECTION

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
RF input frequency	Compatible to IEEE Std.802.15.4-2006, 250 Kbps	2405		2480	MHz
RX sensitivity	Measured as defined by IEEE Std.802.15.4-2006 using the given conditions. IEEE Std.802.15.4-2006 requires a minimum sensitivity of -85 dBm		-95		dBm
Maximum RF input			3		dBm
RSSI range			44		dB

RF TRANSMIT SECTION

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
RF carrier frequency	Compatible to IEEE Std.802.15.4-2006, 250 Kbps	2405		2480	MHz
Maximum RF output power	At 0 dBm output power setting		0		dBm
RF output power control range	-40 dBm ~ 0 dBm		40		dB
TX EVM	Measured as defined by IEEE Std.802.15.4-2006 with maximum output power setting. IEEE Std.802.15.4-2006 requires a maximum of 35% EVM		12		%

5. Application circuits

A typical circuit diagram of HB2200 is illustrated in Figure 5-1, where power supply decoupling capacitors and connection of digital I/Os are not shown. Capacitors must be placed as close as possible to each power pin. The crystal loading capacitance should be determined according to the choice of crystal oscillators. When some GPIO pins (among P0, P1, and P2) are not used, they are recommended to be configured as an input pull-up state.

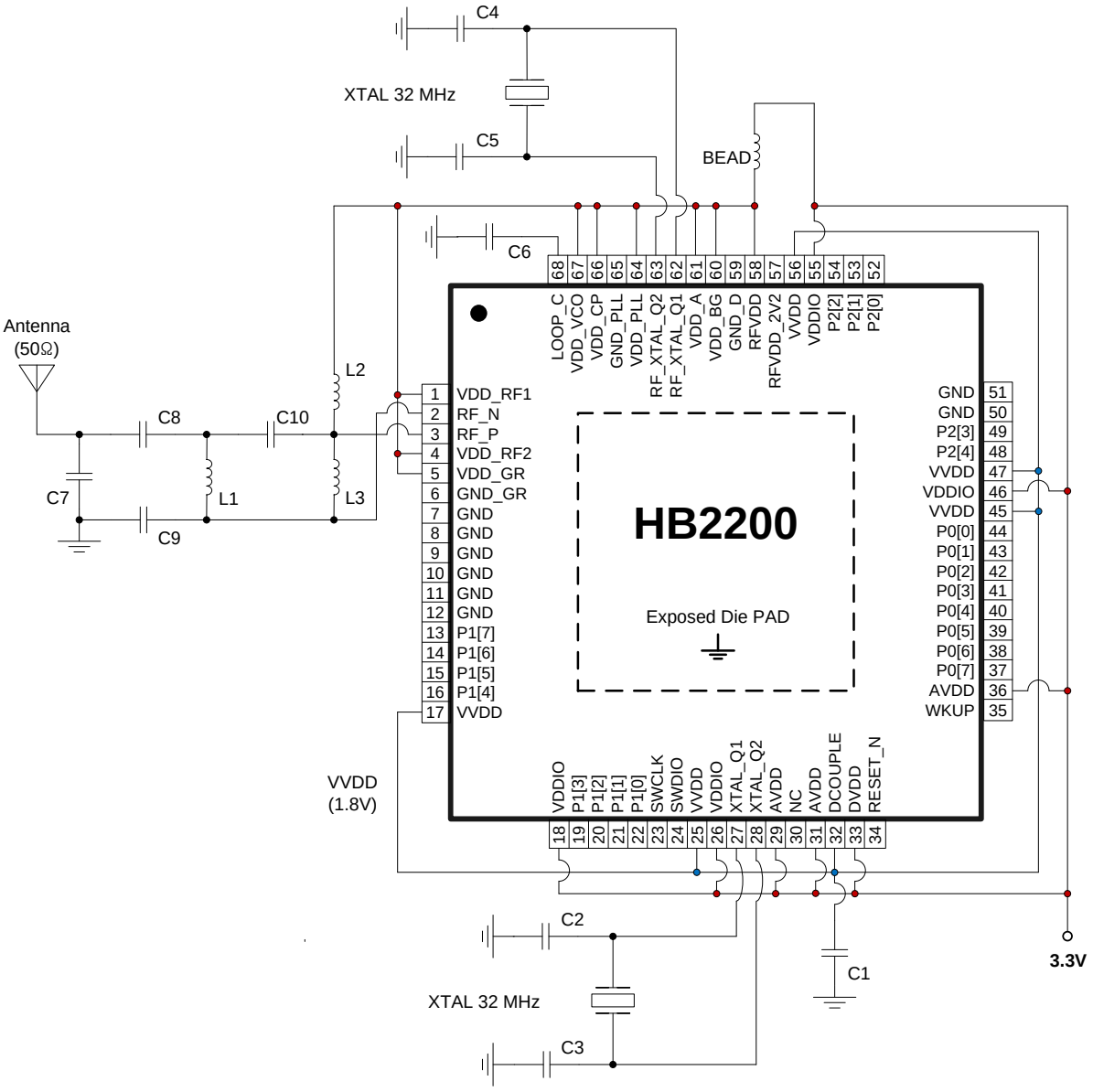

Figure 5-1. A reference application circuit configuration

Table 5-1. Typical values of external components

COMPONENT	DESCRIPTION	VALUE
C1	Decoupling capacitor for 3.3V supply	10 uF, 0.1 uF
C2	32 MHz crystal loading capacitor	10 pF
C3	32 MHz crystal loading capacitor	10 pF
C4	32 MHz crystal loading capacitor for RF operation	10 pF

C5	32 MHz crystal loading capacitor for RF operation	10 pF
C6	RF PLL loop filter external capacitor	39 pF
C7	Part of the RF matching network	0.5 pF
C8	Part of the RF matching network	5.6 pF
C9	Part of the RF matching network	1 pF
C10	Part of the RF matching network	0.5 pF
L1	Part of the RF matching network	4.7 nH
L2	Part of the RF matching network	15 nH
L3	Part of the RF matching network	4.3 nH

6. Package specification

Figure 6-1 and Figure 6-2 illustrate the top/side and the bottom view of HB2200 SoC package, respectively.

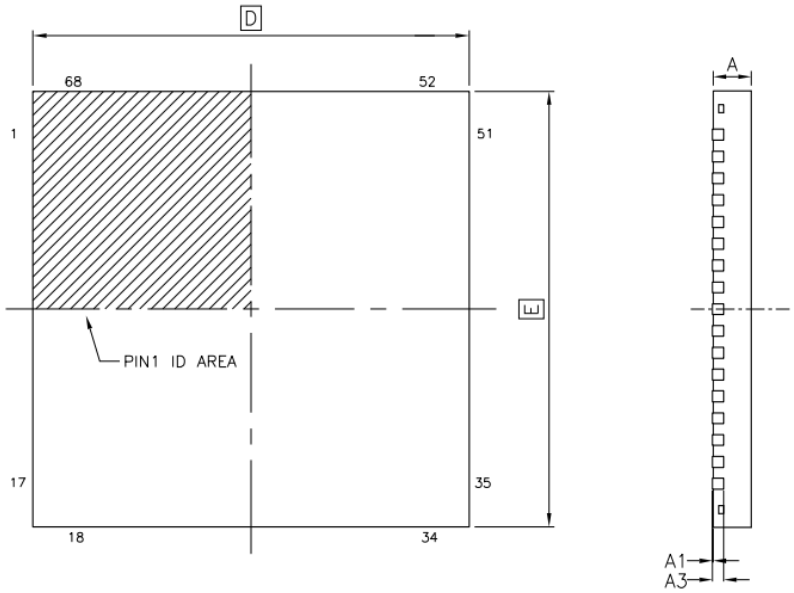

Figure 6-1. Top and side view of HB2200 SoC

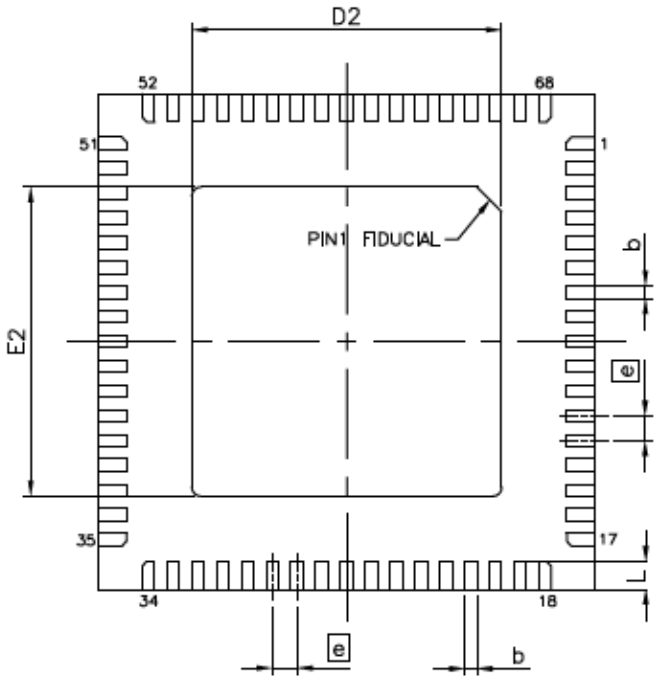

Figure 6-2. Bottom view of HB2200 SoC

Table 6-1 summarizes the common dimensions of HB2200 SoC. Note that the dimension is represented in millimeters.

Table 6-1. Common dimensions of HB2200 SoC

SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.203 REF		
b	0.15	0.20	0.25
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	4.90	5.00	5.10
E2	4.90	5.00	5.10
e	0.40 BSC		
L	0.35	0.45	0.55